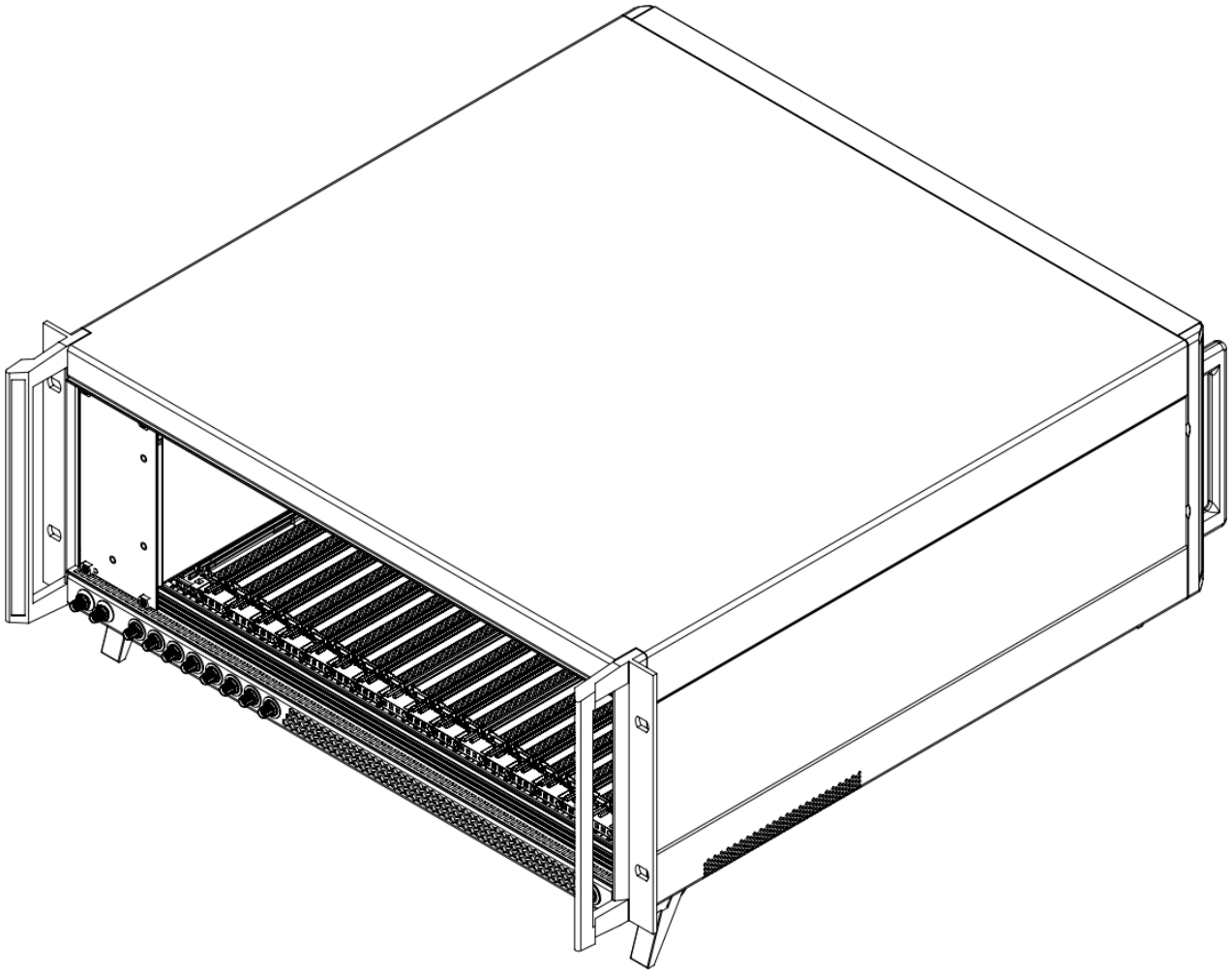
18 Slot PXI Express System 24GB/s

14579-042

User Manual

Release 1.0
16.01.2024



Doc-No: 63972-430

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R1.0	January 2024	Preliminary Release

Table 1: Revision History

Table of Contents

1 Safety

1.1 Intended Use

The nVent SCHROFF PXIe System 14579-042 described in this manual is a high performance 18-slot PXI Express chassis based on an allover fundamental modular design. With this System a new internal hardware concept comes into charge, which is capable to fulfill the highest requirements in card cooling, system bandwidth (up to 24GB/s total and up to 8 GB/s per slot) along with increased system sustainability due to redundant PSU implementation on EMC class B level. The following description of included features and installation guideline shall support a wide range of application cases. Intended use includes compliance with the terms and conditions for assembly, disassembly, commissioning, operation and maintenance, specified by the manufacturer. The PXIe System is only intended for use in dry and dust-free locations, i.e. indoors, in an industrial environment or for commercial use. If the equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.

1.2 Safety Instructions - Disclaimer

nVent SCHROFF accepts no liability for any errors in this documentation. To the maximum extent permissible by law, any liability for damage, direct or indirect, arising from the supply or use of this documentation is excluded.

nVent SCHROFF retains the right to modify this document, including the liability disclaimer, at any time without notice and accepts no liability for any consequences of such alterations.

1.3 Safety Symbols

In these original operating instructions, warning notices point out residual risks that cannot be avoided by constructive means when installing or operating the PXIe System. The warning notices are classified according to severity of the damage occurring and its statistic occurrence.

⚠ DANGER	
Symbol	**Short description of the danger** The signal word DANGER indicates an immediate danger. Non-observance will result in severe injuries or death.

⚠ WARNING	
Symbol	**Short description of the danger** The signal word WARNING indicates a possible danger. Non-observance can lead to serious injury or death.

⚠ CAUTION	
Symbol	**Short description of the danger** The signal word CAUTION indicates a possible danger. Non-observance can lead to injuries.

ATTENTION
Short description The signal word ATTENTION indicates possible damages to equipment. Non-observance can lead to damage to the device.

	**Important information**

1.4 Safety Information for Operators

Only trained specialists are authorized to carry out assembly, commissioning, completion, maintenance and service of the PXIe System. The nationally applicable health and safety regulations must be adhered as well.

⚠ WARNING	
	**Risk of injury due to insufficient personal protective equipment** If you use wrong / no protective equipment at all, serious injuries are possible. - Wear protective equipment adapted to the work processes. - Check the protective equipment before each use to ensure that it is intact! - Use only approved protective equipment.

2 References and Architecture Specifications

2.1 Related Documents

This product meets the requirements of the following specifications:

- IEEE 1101.1-199, including IEC 603-2 Connectors
- IEEE 1101.10, including IEEE 1101.1 Equipment Practice,
- ATX Specification Version 2.4
- PICMG EXP.0 Revision 2.0 CompactPCI Express Specification
- PICMG 2.0 R3.0 CompactPCI Specification
- PXI-1 Hardware Specification Rev 2.3
- PXI-2 Software Specification Rev 2.6
- PXI-5 PXI Express Hardware Specification Rev 1.1

2.2 Electromagnetic Compatibility

The requirements of the following EMC standards for electrical equipment are fulfilled and verified via an independent EMC test laboratory.

- EN 61326-1 class B group 1 — Basic Immunity
- EN 61000-3-3 — Limitation of voltage changes, voltage fluctuations and flicker
- EN 61000-3-2 — Limits for harmonic current emissions

	EN 55011 (CISPR11), EN 55022 (CISPR 22) and EN 55024 (CISPR 24) are implied and in fact fulfilled by EN 61326-1. The international standards AS/NZS (CISPR 11) and AS/NZS (CISPR 22) are also implied by EN 61326-1 and basically fulfilled.

2.3 Safety Certification

The product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control and laboratory use.

- EN 61010-1 / IEC 61010-1

2.4 CE / UKCA Compliance

Essential requirements of applicable European Directives are met by this product. Since 2020 the UKCA declaration requirements are fulfilled as well.

- LVD 2014/35/EU — Low-Voltage Directive
- EMC 2014/30/EU — Electromagnetic Compatibility Directive
- RoHS 2011/65/EU — RoHS Directive 2

Products fulfilling those requirements are marked with a CE/UKCA label.

For Declarations of Conformity of this product please visit **https://SCHROFF.nvent.com/**

3 General Installation

3.1 Unpacking

ATTENTION
When opening the shipping carton, use caution to avoid damaging the system.

Consider the following when unpacking and storing the system:

- Leave the system packed until it is needed for immediate installation.
- After unpacking the system, save and store the packaging material in case the system must be returned.

If the packaging is damaged and possible system damage is present, report to the shipper and analyze the damage.

3.2 Ensuring Proper Airflow

- Maintain ambient airflow to ensure normal operation. If the airflow is blocked or restricted, or if the intake air is too warm, an overtemperature condition can occur.
- Ensure that cables from other equipment do not obstruct the airflow through the system.
- Use the filler panels (included in the delivery) to cover all empty chassis slots. The filler panel prevents air entering at front of an open slot and improves airflow distribution across the chassis
- If necessary, use air baffles (available as accessories) to prevent air short circuits in unused slots.

3.3 Initial Operation

⚠ WARNING	
	**Risk of injury and accidents due to insufficiently qualified personnel!** The installation may only be carried out by qualified personnel who are authorized to do so according to the valid safety regulations, e.g. by authorized specialized companies or authorized departments of the company.

- Ensure that the system has not been damaged during transport, storage or assembly
- Check the Protective Earth (PE) resistance, should be < 0,1 Ohm
- Plug-in the system controller and peripheral boards
- Ensure that all open slots are covered with filler panels or even air baffles
- Ensure that the switch **INHIBIT MODE** at the rear side is set to **DEF**
- Ensure that the switch **FAN SPEED** at the rear side is set to **AUTO**
- Connect **both** power cords to the power inputs of rear PSUs
- Push the power button at the front side to turn **ON** the system and boot up

3.4 Software and Driver Installation

Parametric information of nVent SCHROFF PXI Express chassis is included in a *chassis.ini* description file. Together with EEPROM stored data the used system controller creates a *pxisys.ini* file for the PXI system initialization within OS environment. For the creation of that file the used controller uses PXI-6 dedicated drivers. A complete software package ***(nVent SCHROFF PXIe Initial Setup)*** with essential drivers, system manager tool, INI-files and registry settings is available under following address **https://SCHROFF.nvent.com/en-de/products/enc14579-042** and subchapter “Firmware”

	Before installing the SCHORFF Initial Setup it is mandatory to install a PXI Resource Manager Software Environment, e.g. NI™ Max or Keysight™ Connection Expert.

3.5 nVent SCHROFF System Manager Tool

nVent SCHROFF PXI Express system information can be displayed and managed by the tool **nVent SCHROFF PXIe System Manager**. With the system manager tool all featured chassis functions can be monitored and controlled. For general direct access to chassis management registers all controller based I²C/SMBus interfaces, featured in PXI-6, can be used as well. The registers are described in detail under chapter 7 Chassis Management. For further technical questions, software libraries or example software project, please get in contact with your local sales representative.

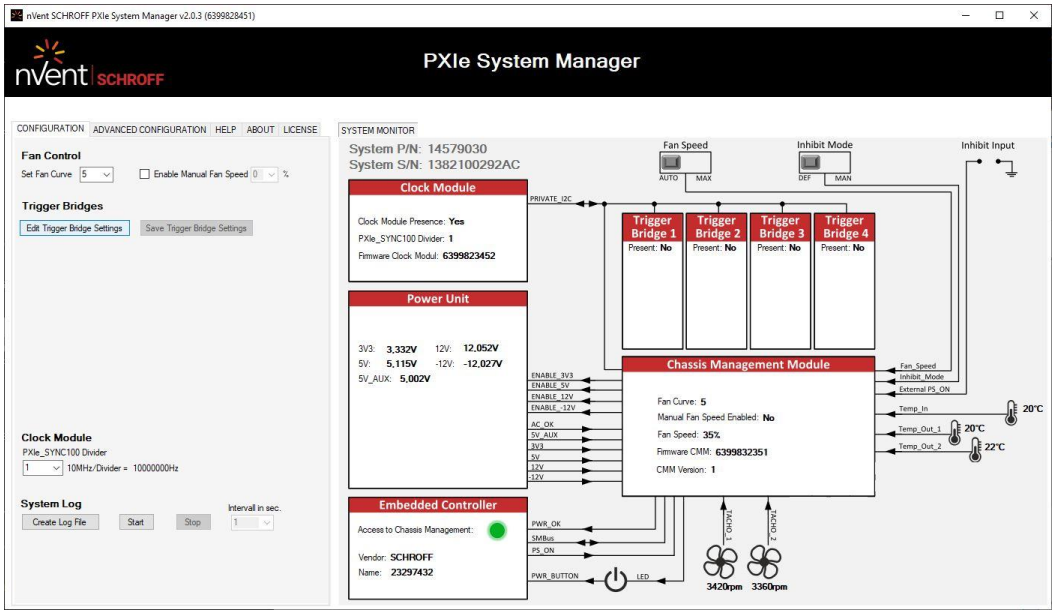


Figure 1: Screenshot PXIe System Manager

4 Technical Information

4.1 Technical Data

The following table provides general technical product information about the nVent SCHROFF PXIe system 14579-042.

Table 2: Technical Data

Dimensions	
Height (w/o feet)	177 mm (4 U)
Height (with feet)	192 mm
Width (with mounting brackets)	84 HP (19“/ 482.6 mm)
Depth (Overall w/o handles)	465,5 mm
Weight	
System without cards and filler panels	12,0 kg
Power Supply	
Input Voltage	100 VAC to 240 VAC (IEC 60320-C14)
Main Supply Voltage fluctuations	10%
Overvoltage category	II
Frequency (nom / operating)	50/60 Hz
Power input	up to 1800 VA (2x 900VA CRPS PSU)
Efficiency	up to 99.0% (full load case)
Overload protection	DC OCP & OVP, AC Fast Fuse
Ambient	
Operation	+0 °C to +55 °C
Storage	-40 °C to +85 °C
Admissible humidity	20 % to 80 %, non-condensing, 2000m
Pollution degree	2
Shock and Vibration	
Shock	15 g peak, 11 ms halfsine EN 60068-2-27
Vibration operation non-operation	5 to 100 Hz, 0,15 g rms EN 60068-2-64 5 to 500 Hz, 1,87 g rms EN 60068-2-64
EMC:	
EMC	EN 61326-1 class B group 1 EN 61000-3-3 EN 61000-3-2
Safety	
Safety	EN 61010-1 / IEC 61010-1

4.2 Key features

The nVent SCHROFF PXI Express chassis 14579-042 is designed for highest performance applications and supports a wide range of requirements due to its modular base structure. The well balanced combination of a performant and redundant dual power supply capable of 1800W , the high bandwidth PCI Express switch architecture (bandwidth up to 24GB/s total and up to 8 GB/s per slot) and the full PXI-1/CPCI downwards compatibility combined with access to all featured chassis functionalities provides customers a platform for the highest demands and usability. The nVent SCHROFF PXIe Chassis meets the high grade quality requirements for advanced timing, synchronization and trigger signals.

The underlying modular design impresses with flexibility and reliability at once due to deeply verified standard function modules and enables the customer to operate a system with lowest failure rate and high maintainability.

- Shielded 4 U SCHROFF ratiopacPRO-air case with mounting brackets for 19“ rack mounting, front handles and tip-up feet for desktop use
- 84 HP / 18 slot front card cage for 3 U boards
- compatible for PXI-5 as well as PXI-1, CompactPCI and CompactPCI Express cards
- 18 slot 3 U backplane containing:
  - 1 PXIe system slot, 4 - 16 HP
  - 1 PXIe timing slot, 4 HP
  - 16 PXI Express Hybrid slots, 4 HP
- System Bandwidth up to 24 GB/s (x8 x16 Port Configuration)
- Up to 8 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-3 PCI Express) grouped within four PCIe switch segments
- SMA connectors for 10 MHz clock input/output at the front side
- 8x configurable (Open/In-/Output) SMA connectors for trigger segment [7:0] at front
- Low Jitter Performance for CLK10, CLK100, SYNC100 signals with featured SYNC_CTRL functions
- PXI_STAR and PXIe_DSTAR[A:C] signals matched in propagation delay to all slots
- Removeable Rear Casset for easy access and maintenance infield and low off-time
- Dual redundant power supply (2x 900 W) with wide range input at EMC class B
- Two Power input module with IEC 60320-C14 connector containing filters and fuses
- 3x 120 mm powerful Fans for cooling control & monitoring via Chassis Management
- Push Button with chassis status indicator LED at front side

	This user manual describes features and system characteristics of the 14579-042 system. The technical description may also apply to customer-specific systems that are based on this manual.

4.3 Front and Rear View

The 4U case is based on the nVent SCHROFF ratiopacPRO-air system with EMC shielding. The 3 U card cage provides 1 system slot (4- 16 HP), 1 timing slot (4 HP) and 16 peripheral slots (4 HP). The lower guide rails of the card cage are equipped with ESD clips.

Figure 2: Front and Rear View

1	Push Button with System Indication LED	**7**	VMON Connector, DSUB-9
2	Filler Panels 4+8HP System Slot Extension	**8**	2x HotSwap CRPS PSUs, IEC 60320-C14
3	PXIe Slots guiding for Card Insertion	**9**	Fans / Air Outlet
4	Air Intake (Front, Bottom)	**10**	Fan Mode Slide Switch
5	2x CLK10_IN / _OUT connectors, SMA	**11**	Power Mode Slide Switch
6	8x Trigger Line [7:0] connectors, SMA	**12**	Grounding stud (M5)

4.4 Interchangeable Components

With an in-depth modular hardware platform the system 14579-042 is divided into a signaling area, consisting of backplane including all functioning modules (please refer to chapter 4.6), and an area containing supply infrastructure like power distribution, fans, plug-in power supply units and miscellaneous. Both areas are separated by an EMC shielding. The rear cassette contains active power distribution, three powerful fans, the rear panel with switches for system modes and can support two hot-swappable PSUs. It can be inserted from the rear of the system via two Teflon guides and is securely connected to the housing via 5 fixing screws on the rear panel. For the dedicated system it is delivered with two interchangeable CRPS PSUs, which are working a load sharing parallel mode. Thus they can be used in fail-over scenarios and are providing a (n-1) redundancy characteristic when used correctly (please refer to chapter 4.7).

⚠ WARNING	
	**Risk of injury and accidents due to insufficiently qualified personnel!** The installation may only be carried out by qualified personnel who are authorized to do so according to the valid safety regulations, e.g. by authorized specialized companies or authorized departments of the company.

To replace the rear cassette (1) or the power supply units (2), please follow the safety instructions along with the detailed installation instructions supplied with the respective spare part. For more information to spare parts please refer to chapter 8.5 or get in contact with your local sales representative.

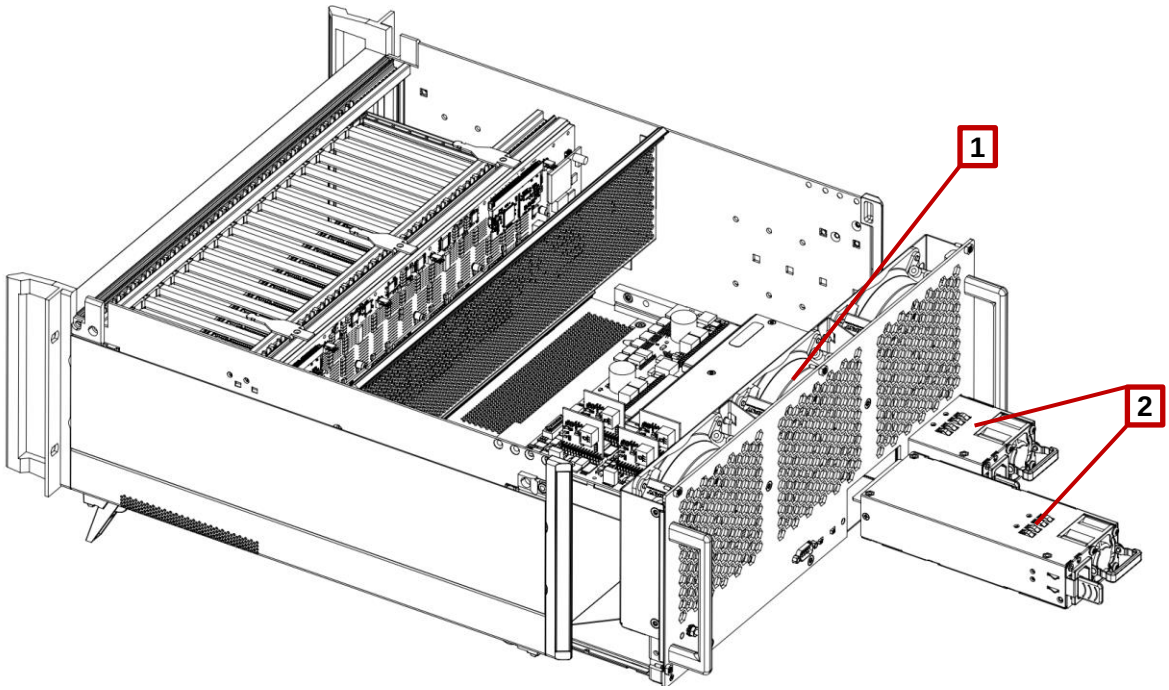


Figure 3: Interchangeable Sub components

4.5 Signal Architecture

The PXI Express system and backplane provides following slots and signal architecture:

- **PXI Express System Controller Slot (Slot 1)**

  The System Slot is a 2 port (x8 x16 Gen3) configured host interface for the usage of PXI Express and Compact PCI Express based controller or adapter cards. The System Controller can have a physical width between 4-16 HP. Each PCIe port of the System slot is connected to a PCI Express switch fabric module distributing PCI Express further ports to the peripheral segments. The max. total bandwidth (single direction) is up to 24GB/s in total and 8GB/s to and between each peripheral endpoint. In addition the switch inner segmental bandwidth is optimized for clustered applications due to flexible packet flow control and does not affect the upstream / CPU performance.

- **PXI Express System Timing Slot (Slot 10)**

  The System Timing Slot can either be used with an CPCIExpress / PXI Express Peripheral Card or and a dedicated PXI Express System Timing Module up to x8 Gen3 PCI Express. When the PXI_CLK10_TS pin of the timing slot is used, the linked to clock module will be phase locked and use the System Timing Slot as reference for enhanced clock quality or synchronization. The PXI_STAR and DSTAR signal groups are all matched in propagation delay and connected in star-shape to all slots according to PXI-5.

- **PXI Express Hybrid Peripheral Slots (16x Slots, Slot 2-9 and 11-18)**

  The 16x PXI Express Hybrid Slots are supported with x8 Gen3 PCI Express Links with up to maximum bandwidth of 8 GB/s single direction and with a 32-bit 33MHz PCI Bus segment connection. The peripheral slots are physically accepting CompactPCI, PXI-1, CompactPCI Express, and PXI Express Peripheral Cards and are providing full PXI Express functionality, as well as the PXI Local Bus.

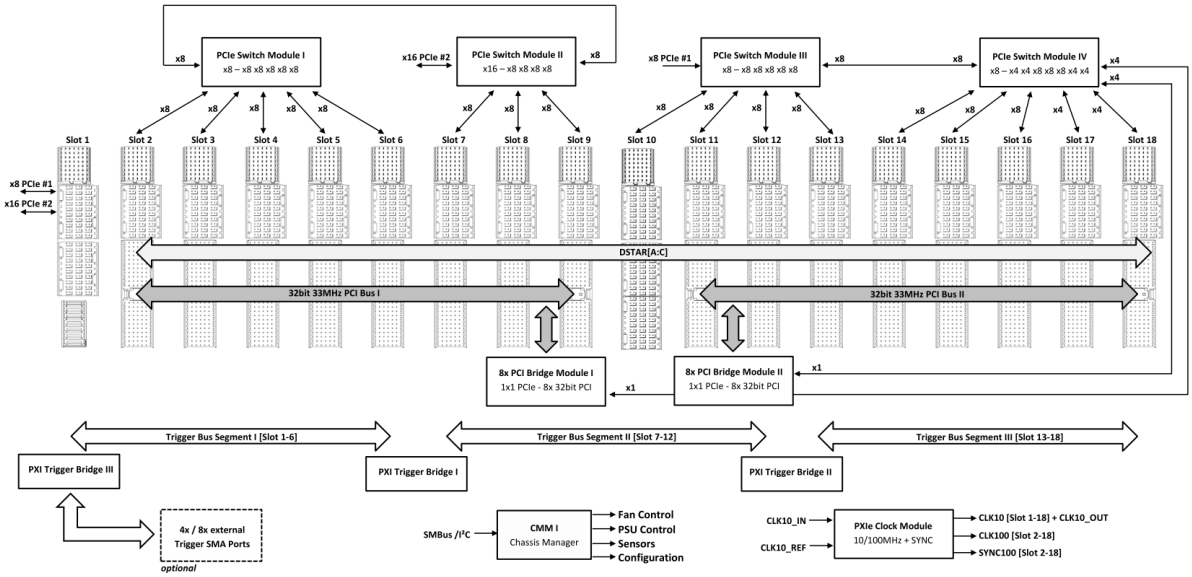


Figure 4: Backplane Topology

4.6 Functional Modules

4.6.1 PCIe to PCI Bridge Module

The nVent SCHROFF PCIe-to-PCI Bridge is a performant bridge designed in accordance to the PCI Express-to-PCI Bridge Specification 1.1 enabling applications to migrate legacy parallel PCI bus interfaces to the advanced serial PCI Express. The bridge module is equipped with a single lane PCI Express port and a parallel bus segment supporting the conventional PCI operation for up to eight PCI peripheral devices concurrently.

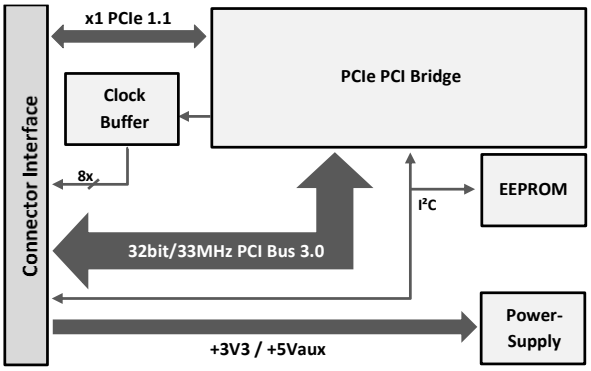


Figure 5: PCIe to PCI Bridge Module

4.6.2 PCIe 48 Lane Switch

The nVent SCHROFF PCIe Switch is a 48-lane, 6-port (up to 12) , PCIe Gen 3 switch device that enables users to connect a PCI Express host to respective endpoints via a fully transparent, high-bandwidth, non- blocking peer-to-peer interface. The default configuration with up to x16 Gen3 PCI Express upstream port to the host supports up to 12 ports distributed on the 48 lanes. For further information (e.g. custom configuration) or SI reports feel free to contact your local sales partner. Default configuration is addressed according to backplane signal topology.

Port Configuration: 48 Lanes configurable in up to 12 ports x16/x8/x4 PCI Express Gen3
Compatibility: PCI Express Base Specification R3.0, PCI Express Base Specification R2.0, PCI Express Base Specification R1.0a/1.1

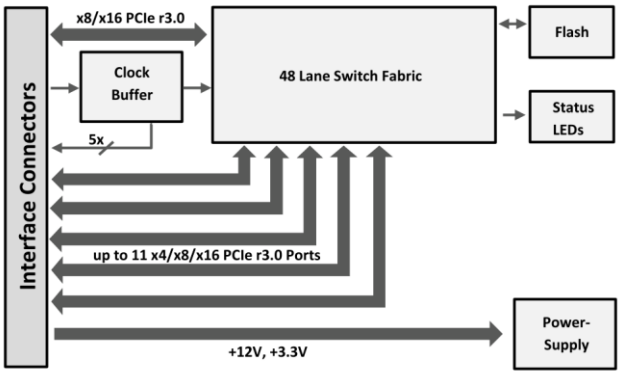


Figure 6: PCIe 48 Lane Switch Module

4.6.3 Clock Module

According to PXI-1 and PXI-5 specification, the nVent SCHROFF PXIe system provides time correlated signal groups PXI_CLK10 and PXIe_CLK100 / PXIe_SYNC100. PXI_CLK10_OUT is also attached to an external BNC connector 10 MHz REF OUT at the chassis rear side.

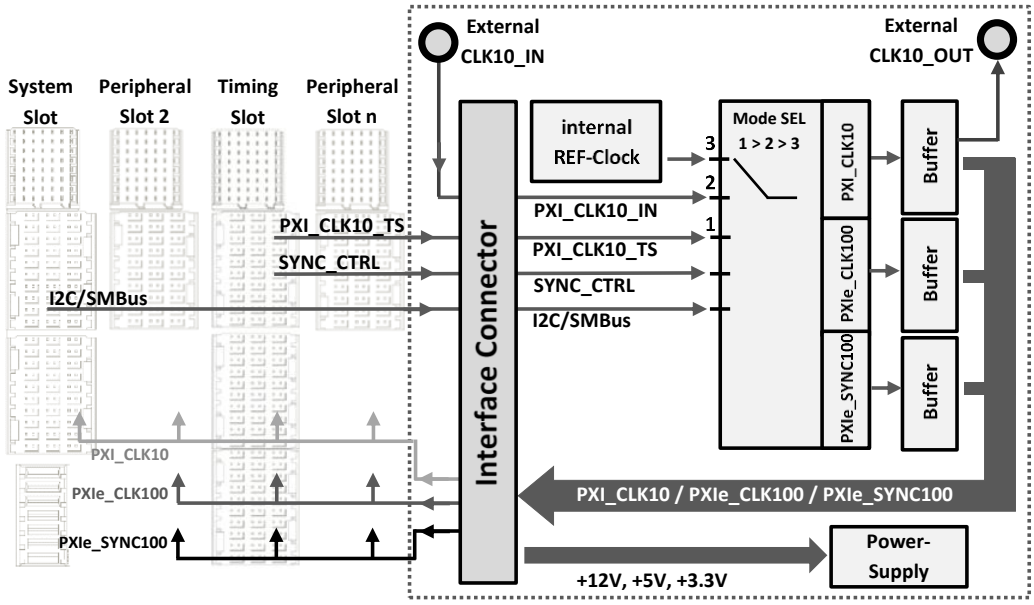


Figure 7: Clock Module

Clock source selection, signal generation and all timing correlations are managed by an clock module, described in the shown block diagram. When a 10 MHz reference clock is present at the System Timing Slot or the external panel connector CLK10_IN, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are phase-locked to this reference clock signal according to chapter 6.3.

4.6.4 Trigger Bridge

For best signal behaviors and low bus capacity a trigger bus shall be limited for up to eight trigger devices according to PXI-1. Trigger buses exceeding slot counts are divided into several individual trigger segments and can be connected unidirectional into both directions via trigger bridges. Trigger bridges are configured by the Host PC or direct I2C/SMBus access. Upon power cycle the last valid trigger configuration is reloaded by the trigger bridge.

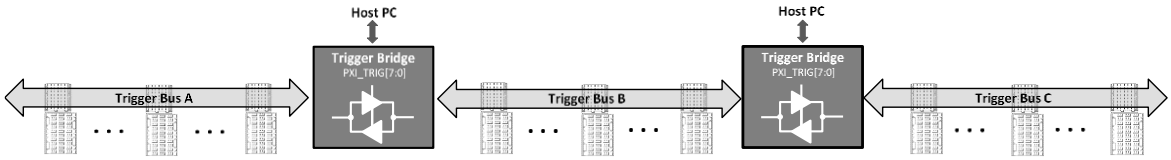


Figure 8: Trigger Bus Segments

Each segment is fully terminated on both ends for optimized trigger performance, even external trigger feed in/out is possible with custom trigger bridge architecture. For further information (e.g. custom configuration) or SI reports feel free to contact your local sales partner.

4.6.5 Chassis Management Module

The Chassis Management Module (CMM) is dedicated to manage all functions of the chassis. The block diagram below shows the management architecture of the PXIe chassis. The CMM provides access to voltage monitor, FAN settings, temperature monitor, Trigger bridge settings and PXIE_SYNC100 frequency settings. The status of chassis functions can be monitored/changed by access corresponding CMM register settings. The System module connects to the CMM via I2C/SMBus which allows access to its configurable registers from the host operating system. However, it is not necessary to access the CMM in default operation. Upon first use it acts autonomously and can be changed in its behavior if required.

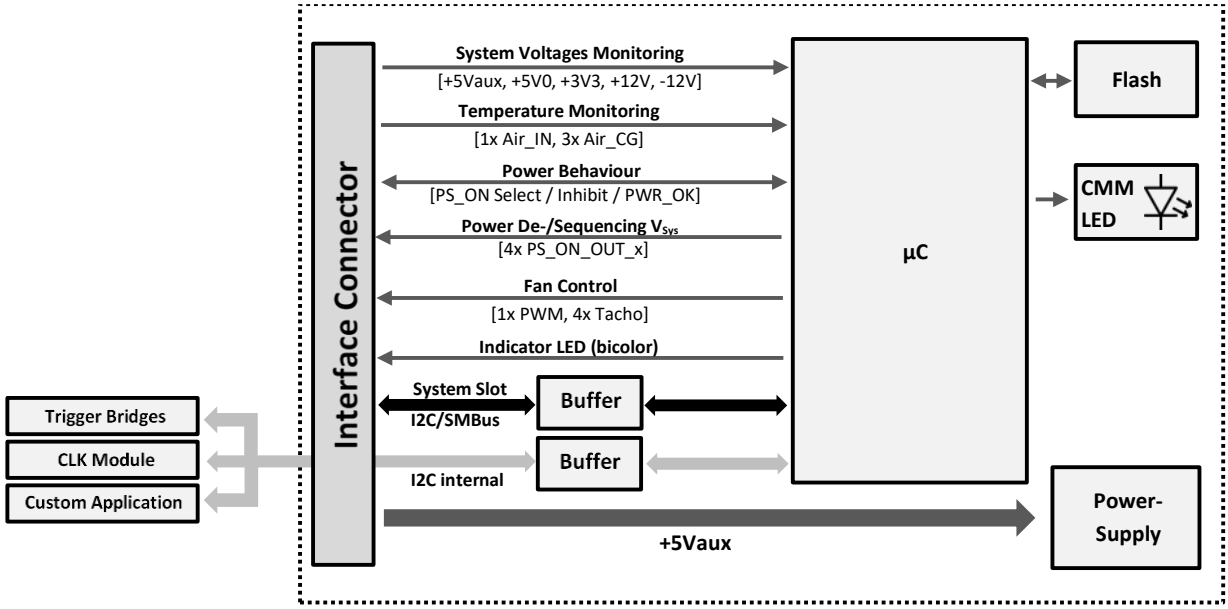


Figure 9: Chassis Management Module (CMM)

4.7 Power Supply

⚠ DANGER	
	**Danger of electric shock** Parts of the power supply may be exposed with hazardous voltage. Always remove mains/line connector before carry out any assembly work.

⚠ CAUTION	
	**Danger of overheating** Your system has not been provided with a AC power cable. Purchase AC power cables that is approved for use in your country. The AC power cables must be rated for the product and for the voltage and current marked on the product's electrical ratings rear. The voltage and current rating of the cable should be greater than the ratings marked on the product.

The PXI Express system 14579-042 is powered by two independent high efficiency CRPS power supplies with wide range AC input.

Input voltage nominal	100 - 240 VAC			
Mains Frequency	50 / 60 Hz			
Power (max. combined)	1800 W	(2x 900W)		
System Voltages	**Voltage**	**Current**	**Load Reg.**	**Ripple**
	+3.3 V	65 A	±5 %	±50 mV
	+5.0 V	30 A	±5 %	±50 mV
	+5.0 Vaux	3 A	-	±50 mV
	+12.0 V	125 A	±5 %	±100 mV
	-12.0 V	2 A	±5 %	±100 mV

Table 3: Input and Output Voltages

The PSU AC sockets provide an power input with IEC 60320-C14 connector and integrated mains/line fuses and line filters. Both CRPS power supplies are using a fast blow type AC Line fuse and is capable of <35 A initial current surge (<10 ms) at cold start. For further information on PSU, custom assembly options or EMC reports please contact your local sales partner.

4.7.1 Redundant Hot-Swapable CRPS PSUs

The system is applied with two CRPS PSUs which are able to load share in parallel mode and operate in a hot-swap / redundant configuration. The load sharing is active from 5% of full load. The failure of a power supply will not affect the output voltages of the other supply still operating . When the AC supply to each PSU C14 connector comes from an independent AC grid the system availability can be increased to a N-1 redundancy. If only one of both power supply units is active, the system supply can be provided for only up to 900W.
For further information on spare parts please refer to chapter 8.5.

4.7.2 Maximum Slot Current Carrying Capability

The table below shows the maximum available current per voltage per slot type. Limiting factors are the maximum current per connector, overall load distribution and available cooling depending on the installed board air impedance and electrical power.

Please note:

- All current carrying backplane pins must be used by the boards
- Do not exceed max. per slot cooling capacity (please refer to chapter 4.8)

Table 4: Maximum Slot Current Carrying Capability

	+5.0V	+3.3V	+12V	-12V	+5Vaux
PXI Express System Controller Slot	10.5 A	10.5 A	21 A	0 A	1.5 A
PXI Express Peripheral Slot Type 2	0 A	4.5 A	3 A	0 A	1.5 A
PXI Express Hybrid Slot	12 A	19.5 A	4.5 A	1.5 A	1.5 A

4.7.3 Chassis Grounding

⚠ CAUTION

The unit is designed in accordance with IEC320 protection class 1! It must therefore be operated with protective earth/GND connection. Use only a three conductor AC power cable with a protective earth conductor that meets the IEC safety standards!

The PXI Express system provides an additional ground terminal at the rear side panel. If necessary, an additional protective ground cable can be connected to the bolt. Please make sure that an appropriate sized cable cross-section is used for this purpose.

4.7.4 Power-On / Power-Off Behavior

When the chassis power mode switch is set to **'DEF'**, the Chassis Management controls the power supply inhibit, which means, the chassis can be powered on and off by pushing the power button at the right front side. When the inhibit mode switch is set to **'MAN'**, the chassis boots when AC-power is applied, as long as Pin 5 at the DSUB connector is not connected to GND. During Power-On and -Off DC voltages are de-/sequenced, see 7.4.5.

4.7.5 Voltage Monitoring

Voltages are measured and controlled by chassis management and can be accessed by a rear D-SUB 9pin connector, see 5.4. When the measured system voltages are exceeding the 5% tolerance according to based on ATX specification for >1 sec the system will provide DC shutdown and the LED will keep flashing red, see 5.1, until an AC power cycle (G3) is applied.

4.8 System Cooling

The PXIe boards are cooled by forced air convection with three controlled 12 VDC axial fans. The air enters the subrack at the perforated bottom panel into the bottom air plenum. As the air passes across heat sources along the peripheral boards, heat is carried away by forced convection. The air exits the cardcage at the top, is drawn into the upper plenum, turns 90°, passes the modules located at the backplane‘s rear side and is exhausted out the rear of the chassis by three fan openings. The cooling capacity of the PXIe chassis can handle nominal **80 W** peripheral cards over complete operation temperature span. For more details to air distribution and cooling capacity, please refer to chapter 4.8.2. The actual heat dissipation for a specific slot depends on the pressure drop of the card used and the occupancy of the adjacent slots. For high performance cards, the slot with the highest air flow should be used and the air leakage (see Fig. 12) of adjacent slots or minor blocked slots should be reduced by air baffles or other air impedance corrections.

	Generally specific applications slot with higher per slot power requirements or low noise requirements are possible and should be discussed in detail based on application in close contact with our engineering department. Please contact your local sales partner for more information.

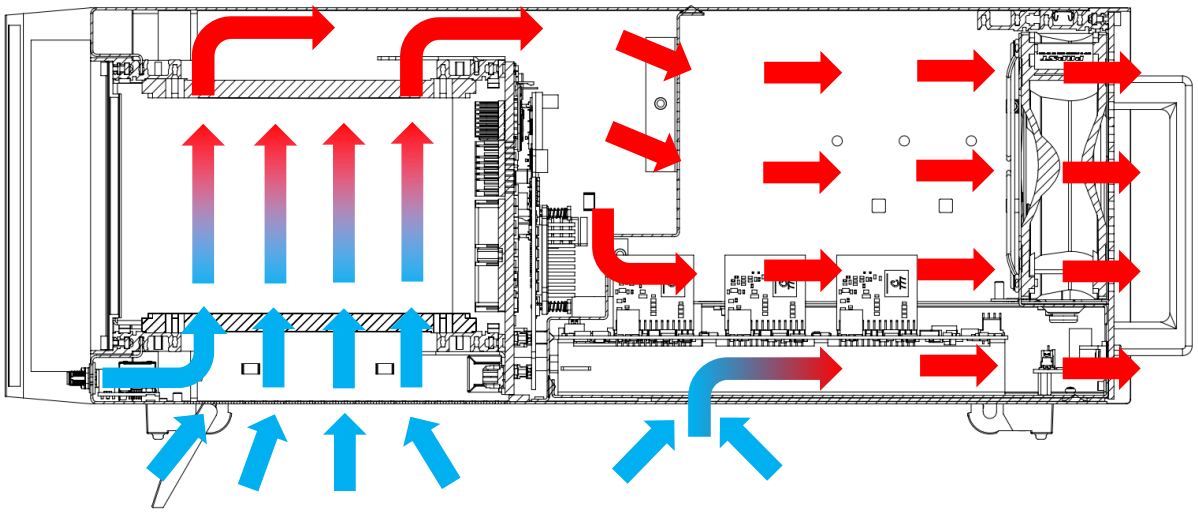


Figure 10: Air Flow

4.8.1 Air Flow Analysis

The following air flow analysis performed with the test system 14579-042 and the nVent SCHROFF air performance test setup. Air flow measurement of the 18-Slot PXIe (14579-042) was performed @ 100%, 90%, 80%, 70%, 60%, 50%, 40% and 30% fan speed. The PXIe chassis was fixed at an air performance test rig. During the test procedure the system was equipped with dummy impedance boards to simulate real chassis setup conditions. These Dummy Impedance Boards consists of a PCB with an obstruction on the top side, which is defined for an 50% air blockage within the 4TE wide air channel.

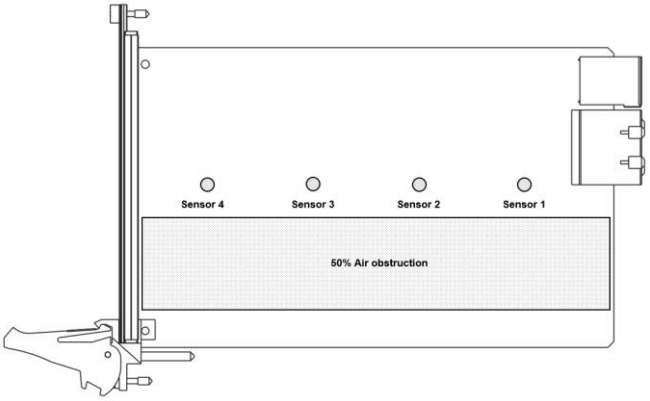
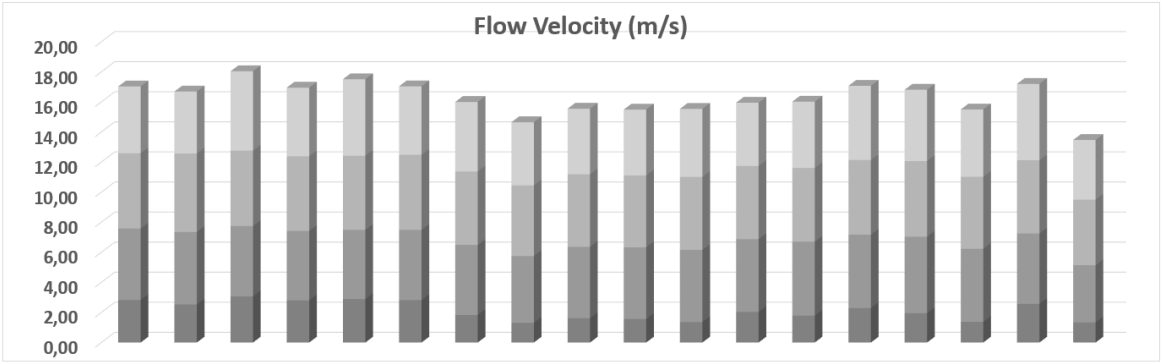


Figure 11: Dummy Impedance Board

The value of 50% is empiric and varies under real application conditions in accordance to the used peripheral cards into uneven populated blockage setup with more or less blockage at each slot. The following measurements shall be used as a well evaluated data base for further integration considerations.

4.8.2 Air Distribution



	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12	Slot 13	Slot 14	Slot 15	Slot 16	Slot 17	Slot 18	Ø
sensor 4	2,83	2,53	3,07	2,80	2,89	2,82	1,83	1,31	1,62	1,56	1,36	2,03	1,79	2,29	1,95	1,37	2,57	1,34	2,11
sensor 3	4,75	4,82	4,67	4,62	4,60	4,67	4,66	4,44	4,74	4,77	4,80	4,84	4,91	4,88	5,08	4,86	4,68	3,80	4,70
sensor 2	5,01	5,22	5,02	4,96	4,93	4,99	4,88	4,70	4,83	4,78	4,85	4,87	4,91	4,97	5,04	4,79	4,87	4,36	4,89
sensor 1	4,44	4,12	5,28	4,57	5,09	4,56	4,63	4,20	4,36	4,38	4,53	4,21	4,41	4,93	4,74	4,48	5,08	3,97	4,55
total airflow [m³/h]	17,03	16,69	18,04	16,95	17,51	17,04	16,00	14,65	15,55	15,49	15,54	15,95	16,02	17,07	16,81	15,50	17,20	13,47	78,79
cooling capacity [W]	103,21	101,15	109,33	102,73	106,12	103,27	96,97	88,79	94,24	93,88	94,18	96,67	97,09	103,45	101,88	93,94	104,24	81,64	98,49

ΔT [Kelvin] 20,00

air volume flow slot 1-18	292,57	m³/h
air volume flow free expansion slots	46,30	m³/h
total air volume flow	338,87	m³/h

Figure 12: Air Distribution

All measured sensor air flows are summed up and used as a per slot air velocity. The assigned slot cooling power is defined on ΔT =20 K temperature increase from air inlet to outlet temperature. The homogeneous air impedance along the above testing should be used as a better understanding for higher integrative system designers. Cooling effects may vary significantly upon the realistic air impedance derivation, resulting total impedance and correlated working point of fans and other effects. With an overall 50% blockage within peripheral cards the system fans can apply a total pressure of 242 Pa, which can vary in countercorrelated dependency to total system air impedance. In allowance of a reduced operation temperature range (e.g. 0-40°C) the fan speed and resulting noise or the cooling capacity per slot (>100 W per slot) can be enhanced upon applicational needs.
For a close technical project support (design approval, thermal simulation, air performance testing and reporting) please get in contact with your local sales partner.

ATTENTION
Danger of Overheating To maintain proper airflow, all open slots must be covered with filler panels. The filler panel should include an airflow baffle that extends to backplane. For desktop use, unfold the front tip-up feet for optimal cooling efficiency. For rack mounting, at least 1 U (44.5 mm/1.75 in.) clearance below the chassis is required.

4.8.3 Temperature Settings

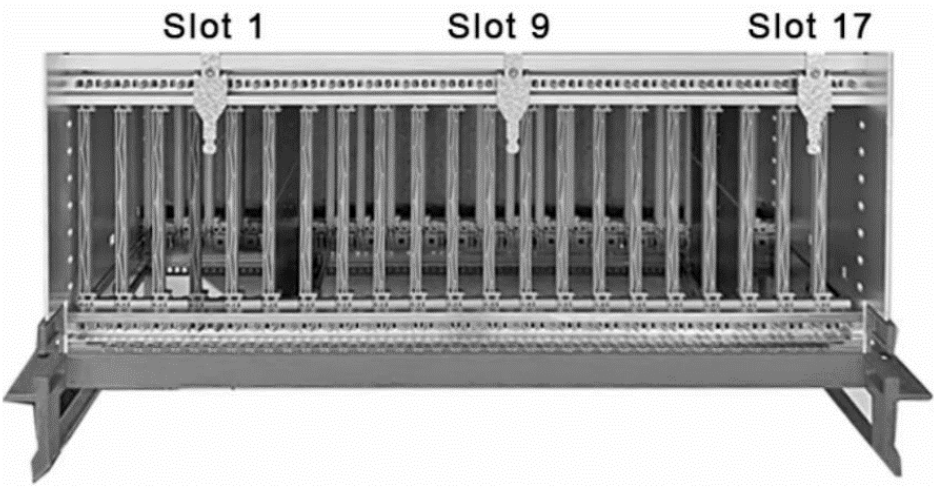


Figure 13: Temperature Sensors

3 NTC temperature sensors located in top of the card cage are monitored by the chassis management. The highest temperature level is the referred control parameter for the overall fan speed.

	To ensure proper fan control, place the PXIe Modules with the highest heat dissipation in the slots directly underneath the NTC temperature sensors (Slot 1, 9, 17).

The fan speed is controlled by the chassis management depending on a fan level control curve. 16 fan control curves are available and can be selected by the chassis management via host or can be directly written via I2C/SMBus. The default fan curve is “5“. A manual fan speed control or max. fan level via rear switch is also possible. A Temp-Fail event will occur when exceeding +5 K above selected temperature curve maximum (T > 55°C on curve “5”). For more information, see chapter 7.3.3 Fan Control register or 5.2 Fan Modes.

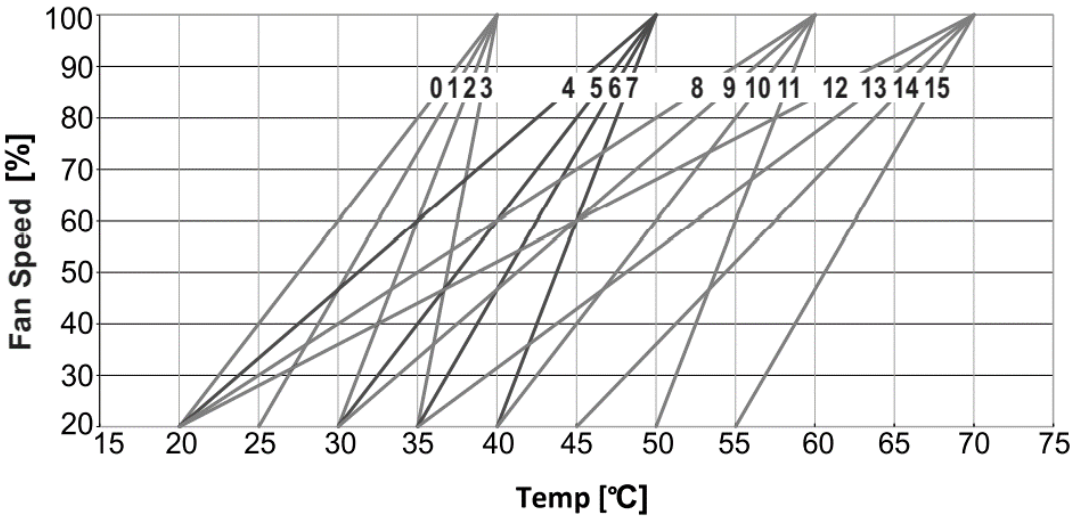


Figure 14: Fan Curves

4.8.4 Options at limited Installation Conditions (blocked bottom air inlet)

For general operation the requirements in chapter 3.2 must be fulfilled. If the installation environment does not correspond to that, general operation of the chassis is also possible for limited conditions **with reduced cooling capacity per slot**. In this case the 4U chassis can be operated with a fully blocked bottom air inlet perforation within an cabinet working height of only 4U. Please make sure that the lower front and side air entrance as well as the rear air outlet is free of any obstacles. Also guarantee that air on chassis front can freely enter the remaining air inlet and is not disturbed by other forced rack air flows.

Within this limited conditions an average cooling capacity of about **35W / slot** (with ΔT =15K) can be assumed without any further airflow restrictions.

	If there is no need for such limited condition, we highly recommend the operation under 3.2 stated conditions for best performance.

For an application evaluated simulation, more detailed information or general application guidance please get into contact with your local sales partner.

4.9 Acoustic Emission

The accoustic emission test was performed under the condition that the PXIe chassis was placed on the test desk. The sound intensity measurement was performed for different fan levels. States between unloaded state (20%) and max. fan level (100%) are described in the following table. Measurements of the sound intensity are performed in accordance to DIN EN ISO 9614-2. Valid for empty Chassis only.

Table 5: Acoustic Emission

Fan Level [%]	**Sound Power L_{WA}** [dB(A)]	**Sound Pressure L_{PA}** [dB(A)] ***0,2m distance***	**Sound Pressure L_{PA}** [dB(A)] ***1,0m distance***
100	79,9	77,0	67,5
90	77,7	74,8	65,3
80	75,7	72,8	63,3
70	72,8	69,9	60,4
60	69,9	67,0	57,5
50	66,6	63,7	54,2
40	62,2	59,3	49,8
30	58,0	55,1	45,6
20	50,5	47,6	38,1

For information about testing procedure and evaluated data contact your local sales partner.

4.10 Mechanical

4.10.1 Materials

Base Materials:

Sheet Aluminium (AW-5754-H22)
Extruded Aluminium (EN-AW-6060 T66)
Plate Aluminium (EN-AW-5005A-H12)
Aluzink Coated (Low Carbon Steel AISI 1008 ASTMA619)
Polycarbonate Lexan
Polyethylene Foam

Finishes:

Color passivated
Clear passivated
Clear anodized
Polyester powder coated
Powder coated fine texture
Painted fine texture

4.10.2 Technical Drawings and Dimensions

Figure 15: Front Isometric View

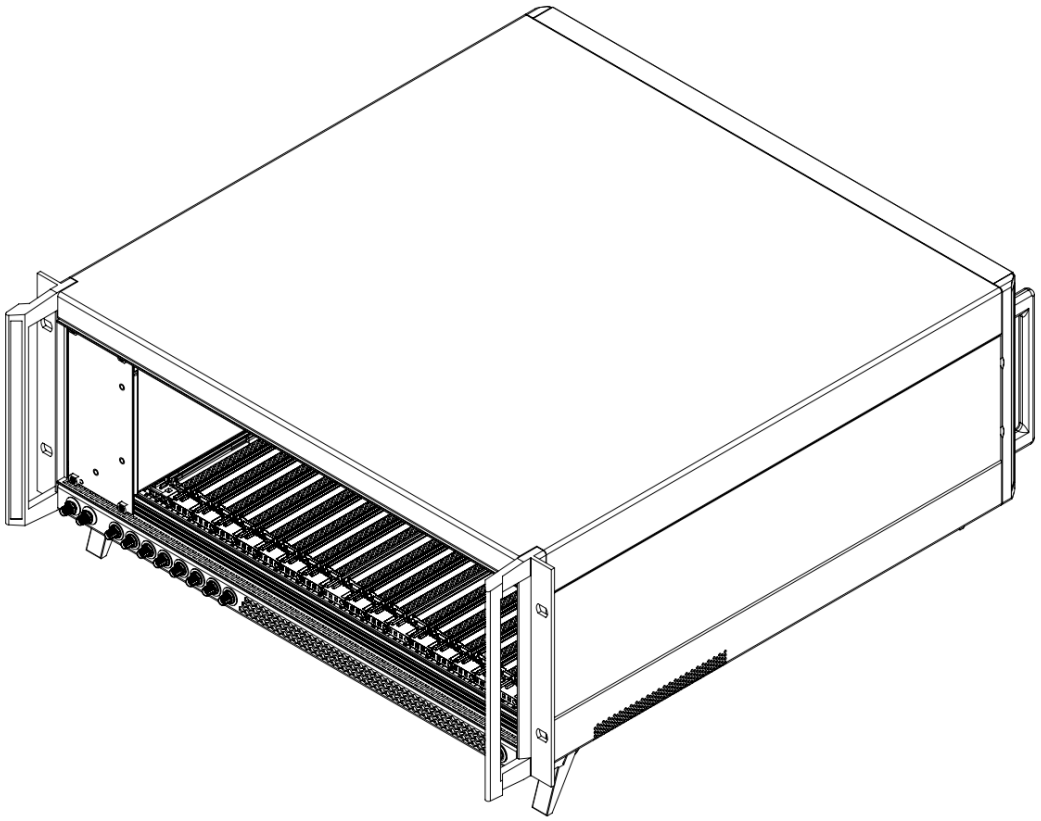


Figure 16: Dimensions Front View

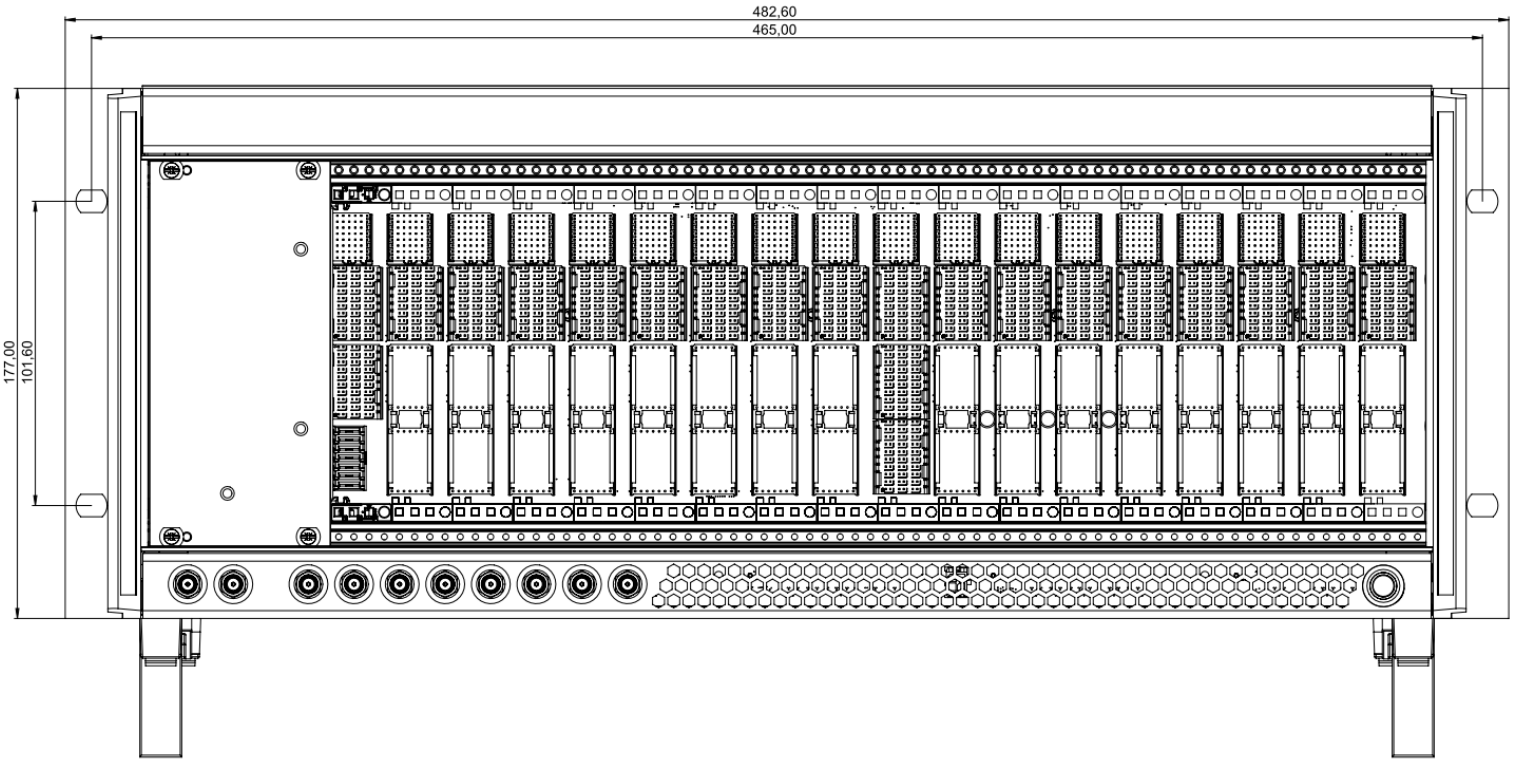


Figure 17: Dimensions Side View

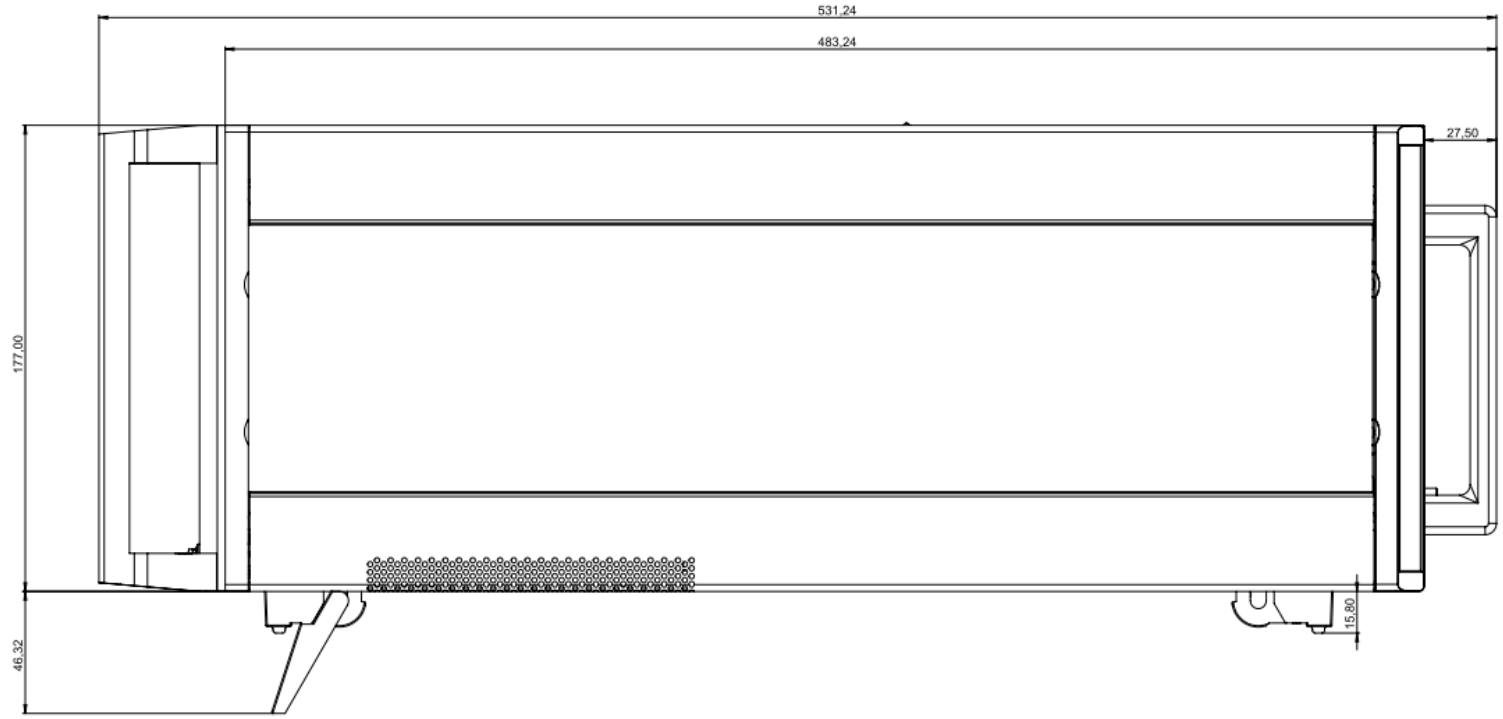
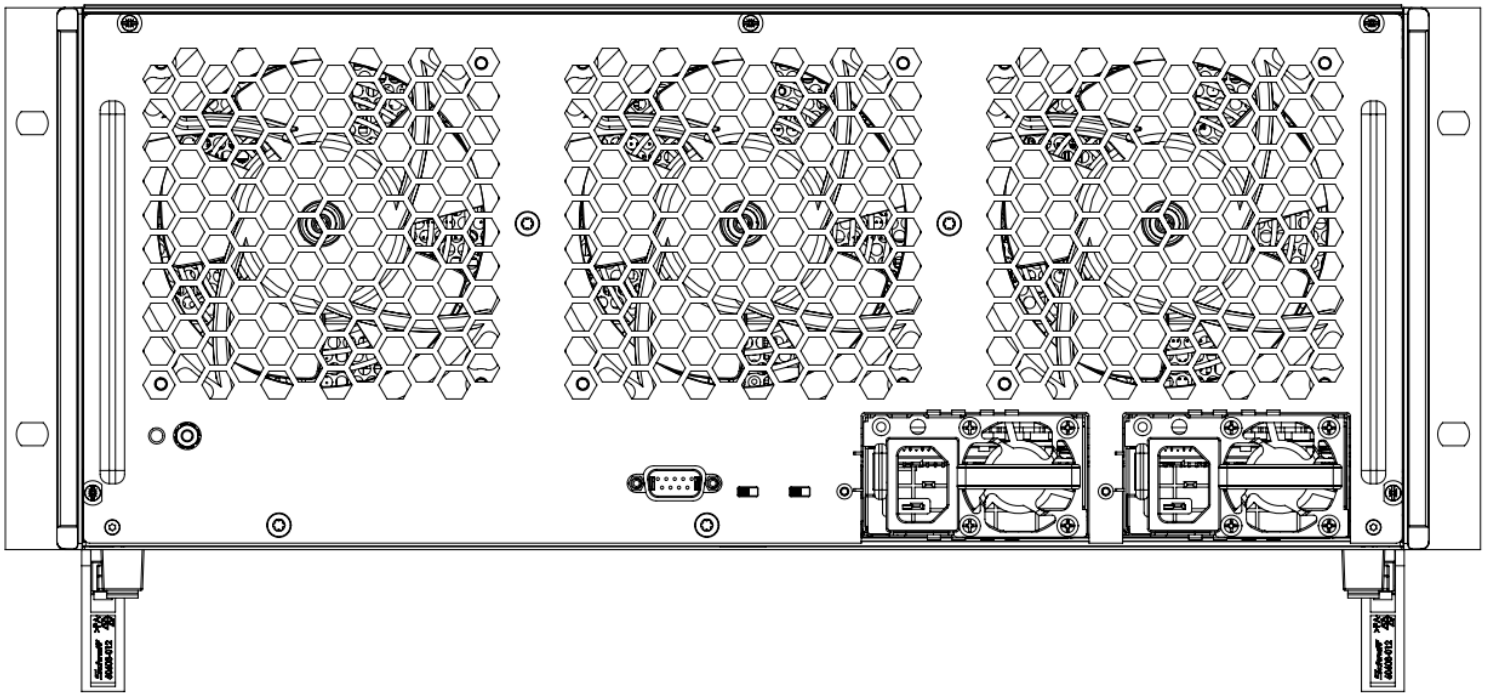


Figure 18: Dimensions Rear View



5 System Status

5.1 Indicator LED

The power switch on the front of the chassis has two integrated LEDs (red and white). CMM signals FRONT_LED_RD and FRONT_LED_WT are used to indicate the chassis status via both of these LEDs. Table below shows the chassis states and corresponding LED behavior.

Table 6: System Status Indicator LED

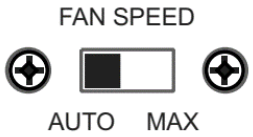
Chassis state	Indicator LED	LED_WT level	LED_RD level
Chassis is off	Both LED OFF	LOW	LOW
Chassis powered and operating properly	Solid white	HIGH	LOW
air intake temperature is above 55°C	Flashing white	Pulse	LOW
One of the chassis fans failed	Solid red	LOW	HIGH
System voltages out of limits	Flashing red	LOW	Pulse

5.2 Fan Modes

Upon the application requirement you can choose either for autonomous fan control or maximum air volume throughput for optimized and remote environments.

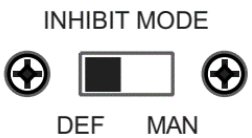
AUTO: Fan Level controlled according to sensor temperature

MAX: Fan PWM set to 100%, Fans run at max. speed



5.3 Power / Inhibit Modes

The power-on behavior depends on the setting of the inhibit mode switch at the rear panel. When the inhibit mode switch is set to "**DEF**", the push button controls the power supply outputs. By pushing the power button at the front side the chassis will start and shut down according to ATX PSU specification 3.2.1.0. When the inhibit mode switch is set to '**MAN**', the chassis boots when AC-power is applied, as long as Inhibit (Pin 5 at the rear DSUB connector) is not connected to GND, please refer to 5.4.



	Please note the following: In order to ensure a proper function of the **DEF** and **MAN** setting, the BIOS settings of the used controller should be adjusted. **DEF Mode:** - Set BIOS Power Loss Control to "Remain Off". **MAN Mode:** - Set BIOS Power Loss Control to "Turn On".

5.4 External Interfaces

CLK10_IN

A BNC rear connector is located at the rear panel and can be used for external clock source input. All chassis clock correlations will follow the external source after the glitch free resourcing. For more information please see chapter 6.3

CLK10_OUT

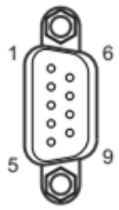
Another BNC rear connector is located at the rear panel and can be used for clock 10 MHz output. For more signal characteristics please see chapter 6.2

DSUB Connector "Voltage Monitor"

All active system voltages are present at a rear 9pin DSUB female connector and can be used for external measurements. With the implementation of the INHIBIT signal multiple chassis applications can be daisy-chained for synced Power-On Behavior.

Whenever the chained **INHIBIT**-Pin is attached to GND potential, System voltages of attached Chassis will be shut down immediately. When **INHIBIT**-Pin is released and Inhibit Mode is set to "**MAN**" system voltages and chassis will power up again.

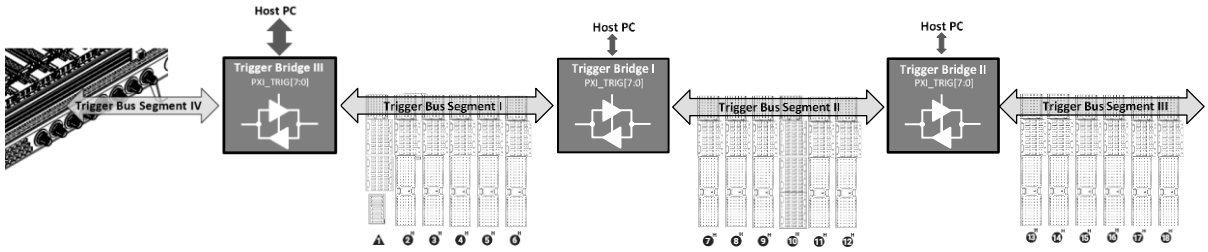
Table 7: DSUB Connector "Voltage Monitor"

	Pin	Signal	Pin	Signal
 VOLTAGE MON	**1**	GND	**6**	+12V (via 10k resistor)
	2	+5V0 (via 10k resistor)	**7**	*not used*
	3	*not used*	**8**	-12V (via 10k resistor)
	4	+3V3 (via 10k resistor)	**9**	GND
	5	INHIBIT		

6 Timing and Trigger Functions

6.1 Trigger and Segments

Figure 19: Trigger Bus Segments



The PXIe chassis trigger bus is divided into 4 isolated trigger bus segments with 8 trigger lines each X_PXI_TRIG[0:7].

- Trigger segment I covers slot 1 through 6
- Trigger segment II covers slot 7 through 12
- Trigger segment III covers slot 13 through 18
- Trigger segment IV covers external trigger lines on front SMA connectors

Through the PXI trigger bridges, each trigger line of a segment can be individually routed in each direction to the according signal of an neighbored trigger segment or be left isolated.

The trigger bridges are controlled by the chassis management and can be set by SCHROFF Software Tooling (see chapter 3.5) or direct SMBus Access (see chapter 7.3.5).

	By default the three trigger bus segments are isolated, the trigger bridges are disabled. The last chosen trigger configuration will be used as trigger setup after a power cycle.

6.2 CLK10, CLK100 parameters

	For all specifications not mentioned in the tables below refer to the PXI-1 und PXI-5 PXIe Hardware specification.

Table 8: PXI_CLK10

PXI_CLK10	
Maximum slot to slot time skew	500 ps Note: PXI-5 spec specifies 1 ns
Frequency accuracy	±25 ppm max (guaranteed over the operating temperature range) Note: PXI-5 spec specifies ±100 ppm
Maximum jitter	5 ps RMS phase jitter (10 Hz 1 MHz range)
Duty cycle	45 % to 55 %
Unloaded signal swing	3.3 V ±0.3 V (LVCMOS driver)

Table 9: PXIe_CLK100

PXIe_CLK100	
Maximum slot to slot time skew	80 ps Note: PXI-5 spec specifies 200 ps
Frequency accuracy	±25 ppm max (guaranteed over the operating temperature range) Note: PXI-5 spec specifies ±100 ppm
Maximum jitter	5 ps RMS phase jitter (10 Hz – 12 kHz, 12 kHz – 20 MHz range)
Duty cycle	45 % to 55 %
Absolute differential voltage when each line pair is terminated with a 50 Ω load to 1.30 V (or Thevenin equivalent)	500 mV to 950 mV (LVPECL driver)

	Values above valid for nVent SCHROFF PXIe standard products. Optimized parameters are available on request (Jitter ≤1 ps, Accuracy 2 ppm, slot-to-slot skew 100 ps)

Table 10: External 10 MHz Reference In

External 10 MHz Reference In	
Frequency	10 MHz ±100 ppm
Input amplitude	200 mV to 5 V, square wave or sine wave
Maximum jitter introduced by backplane	1 ps RMS phase jitter (10 Hz – 10 MHz range)
Rear panel BNC connector input impedance	50 Ω ±5 Ω

Table 11: External 10 MHz Reference Out

External 10 MHz Reference Out	
Frequency accuracy	10MHz ±25 ppm max. (guaranteed over the operating temperature range)
Maximum jitter	5 ps RMS phase jitter (10 Hz – 1 MHz range)
Unloaded signal swing	3.3V ± 0.3V (LVCMOS driver)
Output impedance	50 Ω ±5 Ω

6.3 Clock Source Selection

When a 10 MHz reference clock is present at the System Timing Slot or the external panel connector CLK10_IN, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are phase-locked to this reference clock signal:

Table 12: Clock Source Selection

Mode	System Timing Slot	External CLK10_IN	Backplane Clock Module
1	10 MHz clock present	10 MHz clock present	External CLK10_OUT, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are phase-locked to reference clock signal from **System Timing Slot**
1	10 MHz clock present	-	External CLK10_OUT, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are phase-locked to reference clock signal from **System Timing Slot**
2	-	10 MHz clock present	External CLK10_OUT, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are phase-locked to reference clock signal from **External CLK10_IN**
3	-	-	External CLK10_OUT, PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 are generated **internally** by the **Clock Module Reference Clock**

The source for the reference signal is selected automatically by that default priority order. If no external clock source is present the clock module will generate the required timing signals based on its own source.

6.4 SYNC_CTRL Behavior

The Chassis Management allows to modify the signal “PXIe_SYNC100” behavior by changing the value of “SynDiv” register (see chapter 7.3.6).

PXIe_SYNC100 Modes

- When “SynDiv” register is set to n=2…255, the resulting PXIe_SYNC100 frequency is $\mathrm{PXIe\_SYNC100_{new}} = \frac{10\ \mathrm{MHz}}{\mathrm{n}}$ and the PXIe_SYNC_CTRL signal works as a PXIe_SYNC100 restart initialization (see PXI-5 chapter 4.4.1.4).

- When “SynDiv” register is set to n=0, the PXIe_SYNC100 frequency is 10 MHz and the PXIe_SYNC_CTRL signal works as PXIe_SYNC100 Enable (see PXI-5 chapter 4.4.1.4).

- When “SynDiv” is set to n=1, the PXIe_SYNC100 frequency is 10 MHz and the PXIe_SYNC_CTRL is deactivated.

7 SCHROFF Chassis Management

The nVent SCHROFF PXIe Chassis Management allows access from the operating system directly to all important chassis functions. The Chassis Management Module (CMM) provides an I2C/SMBus interface which is connected to backplane SMB (system slot pins XP3-a3, -b3).

The Chassis Management features:

- Monitors all chassis voltage levels and chassis temperatures
- Monitors and control the power supply and fans
- Controls SYNC100 features from clock module
- Controls the configuration of PXI trigger bridges
- Controls the chassis status LED

The CMM provides access to all important chassis functions (voltage monitor, FAN settings, temperature monitor, Trigger bridge settings, PXIE_SYNC100 frequency settings …). The status of chassis functions can be monitored/changed by access corresponding register settings.

7.1 I2C/SMBus interface description

The CMM provides a primary I2C/SMBus interface connected to the SMB (system slot pins XP3-a3, -b3 and peripheral slots). This Interface allows the host operating system to directly access all important chassis functions. On a decoupled secondary side the CMM interacts with module internal I2C interface, sensors and monitoring.

7.2 I2C Address

PXI-5 specification chapter 4.8 defines an I2C address range for chassis-specific functions.
Allowed addresses are:

58h = 0101 1000b (used as default CMM address)
5Ah = 0101 1010b
5Ch = 0101 1100b

The CMM's address can be changed to above allowed addresses upon request. Please get into contact with your local sales representative.

7.3 Register map:

Chapters below describe the CMM registers and their functions.

Table 13: CMM Register Overview

Register Range [Start / End]		Description	see sub-chapter
0x00	0x09	Voltage Monitoring	7.3.1
0x0E	0x14	Power Control	7.3.2
0x19	0x28	Fan Control	7.3.3
0x2C	0x30	Temperature Monitoring	7.3.4
0x34	0x3C	Trigger Bridge Control	7.3.5
0x45	0x48	Clock Control	7.3.6
0x50	0x58	CMM Software Revision	7.3.7

7.3.1 Voltage monitor registers

Table 14: CMM Voltage monitor registers

Register address	Name	Description	Direction
0x00	5VauxMSB	5 Vaux voltage level (1bit = mV)	Read only
0x01	5VauxLSB		
0x02	3V3MSB	3V3 voltage level (1bit = mV)	Read only
0x03	3V3LSB		
0x04	5VMSB	5 V voltage level (1bit = mV)	Read only
0x05	5VLSB		
0x06	+12VMSB	+12 V voltage level (1bit = mV)	Read only
0x07	+12VLSB		
0x08	-12VMSB	-12 V voltage level (1bit = mV)	Read only
0x09	-12VLSB		

7.3.2 Power control registers

Table 15: CMM Power control registers

Register address	Name	Description	Direction
0x0E	SEL_SS_PS_ON	Shows the current level of CMM input for “PS_ON” source selection slider. Value = 0: signal “EXT_PS_ON_IN” is used as “PS_ON” source Value > 0: signal “SS_PS_ON_IN” is used as “PS_ON” source	Read only
0x0F	SS_PS_ON_IN	Shows the current level of CMM input for “PS_ON” signal from system slot Value = 0: received signal is LOW Value > 0: received signal is HIGH	Read only
0x10	EXT_PS_ON_IN	Shows the current level of CMM input for “PS_ON” signal from external source. Value = 0: received signal is LOW Value > 0: received signal is HIGH	Read only
0x11	PS_ON_OUT_1	Shows the current state of the CMM output “PS_ON_1” Value = 0: output set LOW Value > 0: output set HIGH	Read only
0x12	PS_ON_OUT_2	Shows the current state of the CMM output “PS_ON_2” Value = 0: output set LOW Value > 0: output set HIGH	Read only
0x13	PS_ON_OUT_3	Shows the current state of the CMM output “PS_ON_3” Value = 0: output set LOW Value > 0: output set HIGH	Read only
0x14	PS_ON_OUT_4	Shows the current state of the CMM output “PS_ON_4” Value = 0: output set LOW Value > 0: output set HIGH	Read only

7.3.3 Fan control registers

Table 16: CMM Fan control registers

Register address	Name	Description	Direction
0x19	Remote	0 = CMM controls the fan speed 1 = embedded controller (system slot card) controls the fan speed. This register must be written each 10 seconds with '1' by system controller to stay in Remote control mode, otherwise the CMM folds back to autonomous mode. Default value: 0	Read / write
0x1A	SetFAN	Sets required fan speed for all fans in % (0h = min fan speed, 0x64h = 100% = max fan speed, in remote control only). Default value: 0x64 = 100%	Read / write
0x1B	FAN_curve	Valid in autonomy mode only Fan curve setting Default value: last setting stored in internal EEPROM, factory value = 0x05	Read / write (value stored in EEPROM)
0x1C	FAN_Tacho_1_HighByte	Shows the fan rotation speed. Value in RPM	Read only
0x1D	FAN_Tacho_1_LowByte		
0x1E	FAN_Tacho_2_HighByte		
0x1F	FAN_Tacho_2_LowByte		
0x20	FAN_Tacho_3_HighByte		
0x21	FAN_Tacho_3_LowByte		
0x22	FAN_Tacho_4_HighByte		
0x23	FAN_Tacho_4_LowByte		
0x28	CMM_FAN_ready	Shows that the fans are initialized and ready for operation	

7.3.4 Temperature monitor registers

Table 17: CMM Temperature monitor registers

Register address	Name	Description	Direction
0x2C	TEMP_AIR_inlet	Chassis inlet air temperature sensor. Values and resolution see description below	Read only
0x2D	TEMP_AIR_outlet1	Chassis outlet sensor 1. Values and resolution see description below	Read only
0x2E	TEMP_AIR_outlet2	Chassis outlet sensor 2. Values and resolution see description below	Read only
0x2F	TEMP_AIR_outlet3	Chassis outlet sensor 3. Values and resolution see description below	Read only
0x30	TEMP_AIR_outlet4	Chassis outlet sensor 4. Values and resolution see description below	Read only

Measurement range is defines from 0°C to +80°C
Resolution for all temperature sensors is 1 Kelvin per bit.

Bit [7:0] = temperature value

Examples:

TEMP_AIR_x Value bin	TEMP_AIR_x Value hex	Temperature
0011 0011b	33h	+51°C
0010 0000b	20h	+32°C
0001 0011b	13h	+19°C
0000 0000b	0h	+0°C

7.3.5 Trigger bridge control registers

Table 18: CMM Trigger bridge control registers

Register address	Name	Description	Direction
0x34	TBPres	Trigger bridge present; shows the availability of individual trigger bridges	Read only
0x35	TB1EN	Enables and disables the trigger bridge 1 drivers	Read / write (value stored in EEPROM)
0x36	TB1Dir	Sets the direction of the drivers on trigger bridge 1	
0x37	TB2EN	Enables and disables the trigger bridge 2 drivers	
0x38	TB2Dir	Sets the direction of the drivers on trigger bridge 2	
0x39	TB3EN	Enables and disables the trigger bridge 3 drivers	
0x3A	TB3Dir	Sets the direction of the drivers on trigger bridge 3	
0x3B	TB4EN	Enables and disables the trigger bridge 4 drivers	
0x3C	TB4Dir	Sets the direction of the drivers on trigger bridge 4	

TBPres: Trigger bridge present register:

Bit	7	6	5	4	3	2	1	0
function	Not used	Not used	Not used	Not used	Trigger Bridge 4 present	Trigger Bridge 3 present	Trigger Bridge 2 present	Trigger Bridge 1 present
value	0	0	0	0	X	X	X	X
X = 0: Trigger bridge not available X = 1: Trigger bridge available Default value: not applicable								

TBnEN[1]: Trigger bridge enable register:

Bit	7	6	5	4	3	2	1	0
function	PXI_TRIG7_EN	PXI_TRIG6_EN	PXI_TRIG5_EN	PXI_TRIG4_EN	PXI_TRIG3_EN	PXI_TRIG2_EN	PXI_TRIG1_EN	PXI_TRIG0_EN
value	X	X	X	X	X	X	X	X
X = 0: Trigger bridge driver disabled								

[1] n = trigger bridge number 1 to 4

X = 1: trigger bridge driver enabled Default value: last settings stored in internal EEPROM, factory value = 0x00

TBnDir[2]: Trigger bridge direction register:

Bit	7	6	5	4	3	2	1	0
function	PXI_TRIG7_D	PXI_TRIG6_D	PXI_TRIG5_D	PXI_TRIG4_D	PXI_TRIG3_D	PXI_TRIG2_D	PXI_TRIG1_D	PXI_TRIG0_D
value	X	X	X	X	X	X	X	X
X = 0: bridge sends trigger signals from left to right (from lower to higher backplane slot numbers) X = 1: bridge sends trigger signals from right to left (from higher to lower backplane slot numbers) Default value: last settings stored in internal EEPROM, factory value = 0x00								

7.3.6 Clock control registers

Table 19: CMM Clock control registers

Register address	Name	Description	Direction
0x45	Clockmodule_Present	Value = 0: clock module not available Value > 0: Clock module available	Read
0x46	SynDiv	Controls the “PXIe_SYNC100” behavior and enables the “PXIe_SYNC_CTRL” functionality. Default value: “1”	write
0x47	Clock_SW_revision LOW byte	Clock module software revision	
0x48	Clock_SW_revision HIGH byte		

7.3.7 CMM software revision

Table 20: CMM software revision

Register address	name	Description	direction
0x60-0x69	CMM_SW_revision	CMM module software revision	Read

[2] n = trigger bridge number 1 to 4

7.4 Power Management

The following signals are present on internal PSU_CTRL connector are described for better understanding of power management or as detail information for custom integrations. For further technical information please get into contact with your local sales representative.

7.4.1 SEL_SS_PS_ON (select PS_ON input source)

Input from chassis rear panel switch to CMM. Used to select the source for the **PS_ON** Signal.

- SEL_SS_PS_ON = HIGH
  ➔ backplane system slot is the source for PS_ON (signal **SS_PS_ON_IN**)
- SEL_SS_PS_ON = LOW
  ➔ external source for PS_ON (signal **EXT_PS_ON_IN**)

7.4.2 SS_PS_ON_IN (system slot PS_ON input)

Input from backplane system slot to CMM. When the system slot sets this signal HIGH and the signal **SEL_SS_PS_ON** is HIGH, CMM starts sequential enabling of the +12 VDC, +5 VDC, +3.3 VDC and -12 VDC voltages according to ATX spec.

7.4.3 EXT_PS_ON_IN (external PS_ON input)

Input from external source to CMM. When an external source sets this signal HIGH and the signal **SEL_SS_PS_ON** is LOW, CMM starts sequential enabling of the +12 VDC, +5 VDC, +3.3 VDC and -12 VDC voltages according to ATX spec.

7.4.4 PS_ON_OUT_X (X = [1:4])

When one of the PS_ON inputs (**SS_PS_ON_IN** or **EXT_PS_ON_IN,** depending **SEL_SS_PS_ON**) is high, the CMM sets the individual PS_ON_X outputs HIGH sequentially:

- PS_ON_OUT_1 (used to switch on 5 V)
  Wait 1ms
- PS_ON_OUT_2 (used to switch on +12 V)
  Wait 3ms
- PS_ON_OUT_3 (used to switch on 3,3 V)
  Wait 1ms
- PS_ON_OUT_4 (used to switch on -12 V)

When **SS_PS_ON_IN** or **EXT_PS_ON_IN** (depending **SEL_SS_PS_ON**) is low or a power fail mode is detected the Power Supply will shut down the voltages in accordance to ATX the ATX12V design guide chapter 3.2.10.
"… The +12 VDC and +5 VDC output levels must be equal to or greater than the +3.3 VDC output at all times during power-up and normal operation …"

7.4.5 PWR_OK

The CMM sets the PWR_OK signal HIGH when the +12 VDC, +5 VDC, and +3.3 VDC outputs are above the under-voltage thresholds:

- +3V3 -5% = 3,135 V
- +5 -5% = 4,75 V
- +12 V -5% = 11,4 V

The CMM sets the PWR_OK signal LOW when the +12VDC, +5VDC, and +3.3VDC outputs are below the under-voltage thresholds.

This behavior fulfills the ATX12V design guide chapter 3.3.1 and timing requirements depicted in figure 7.

8 Service

8.1 Technical support and Return for Service Assistance

nVent SCHROFF actively informs their customer about EOL, service expirations and software updates by customer information letters.

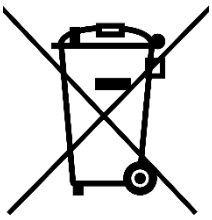
We generally recommend to return the complete system. For all product returns and support issues, please contact your local nVent SCHROFF sales representative to connect you to our technical support team. We recommend that you save the packing material. Shipping without the original packing material will void the warranty.

8.2 Warranty

All nVent SCHROFF hardware features a two-year standard warranty that is extendable upon request. nVent SCHROFF offers repair services performed in a timely manner by highly trained factory technicians.

Declaration of Conformity (DoC)—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product on the corresponding product page on our website **https://SCHROFF.nvent.com/**

8.3 Disposal



The devices described in this manual must be recycled. In accordance with the Directive 2012/19/EC on waste electronic and electrical equipment (WEEE), they may not be disposed of in the municipal waste disposal services. To ensure environmentally friendly recycling the devices can be returned to a locally approved disposal center. Make sure that you observe the regulations applicable in your country.

8.4 Scope of Delivery

Table 21: Scope of Delivery

Quantity	Description
1	ratiopacPRO-air case 4 U / 84 HP, shielded, powder coated
1	PXIe backplane 18 slot 3 U, including: 4x PCIe 48 Lanes Switch 2x PCIe-PCI Bridge 1x PXIe Clock Module 3x PXI Trigger Bridge Modules 1x CMM
2	900 W CRPS power supply with IEC 320-C14 connector (100-240 VAC)
1	Rear Casset with PDB (power distribution, fans and misc)
1	Complete internal wiring
3	Axial fans 120x120 mm
1	Rear panel 3 U, 84 HP

Suitable power cables are sold separately and should be chosen individually.

8.5 Spare Parts and Accessories

Table 22: Spare Parts and Accessories

Order No.	Description
11098-752-SP	CRPS PSU 900W Class B with wide AC input range
24579-638-SP	Rear Casset for 14579042 84TE with 3x 120 Fans, 2 PSU sleds
34562-824	Air baffle 3 U, 4 HP, to prevent air short circuits in unused slots

For more information or quotations, please contact your local sales representative.

8.6 Technical Support for customized solutions

For information about other technical support options, please contact your nVent SCHROFF sales representative. nVent SCHROFF offers modifications and customizations based on our PXI Express Standard Chassis family. Please contact us for your individual requirements. Modifications and customizations include for example:

- color and silkscreen
- mechanical housing
- backplane design
- cooling options
- special requirements for triggers, clocks, in- and outputs

9 Figures

10 Tables